REMARKS

In the Non-Final Office Action, Examiner Shapiro rejected pending claims 9, 10, 12 and 13 on various grounds. The Applicant responds to each rejection as subsequently recited herein, and respectfully requests reconsideration of the present application:

A. Examiner Shapiro rejected pending claims 9 and 10 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,166,715 to *Chang* et al. in view of U.S. Patent No. 5,892,493 to *Enami* et al.

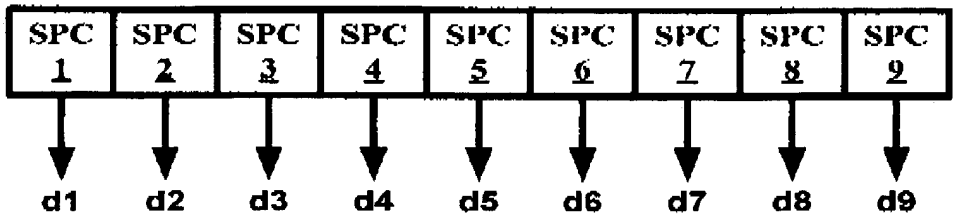
The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of claims 9 and 10 over *Chang* in view of *Enami*. The Applicant has also thoroughly read *Chang* and *Enami*. To warrant this 35 U.S.C. §103(a) rejection of claims 9 and 10, all the claim limitations recited in independent claim 9 must be taught or suggested by the combination of *Chang* and *Enami*. See, MPEP §2143. The Applicant respectfully traverses this §103(a) rejection of claims 9 and 10, because neither *Chang* nor *Enami* disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" as recited in independent claim 9.

As to the traversal, Examiner Shapiro has correctly recognized *Chang*'s failure to teach or suggest the last limitation of independent claim 9. Specifically, as illustrated in FIGS. 3 and 4, *Chang* teaches signal processing circuit 245_1 to 245_{40} where signal processing circuit 245_1 is associated with the first address conductors PIX1, PIX41, PIX81, PIX121, PIX161, PIX201, PIX241, PIX281, PIX321, PIX361, PIX401, PIX441, PIX481, PIX521, PIX561 and PIX601 of groups 1-16, respectively, and where signal processing circuit 245_{40} is associated with the last address

conductors PIX40, PIX80, PIX120, PIX160, PIX200, PIX240, PIX280, PIX320, PIX360, PIX400, PIX440, PIX480, PIX520, PIX560, PIX600 and PIX640 of groups 1-16, respectively. *Chang*'s fails to teach or suggest the last limitation of independent claim 9 by teaching signal processing circuit 245_1 and signal processing circuit 245_{40} are not adjacent as shown in FIG. 3.

Thus, *Enami* must teach or suggest the last limitation of independent claim 9 in order to establish a prima facie case of obviousness. However, Examiner Shapiro has erroneously interpreted *Enami* as teaching the last limitation of independent claim 9, because a proper reading of *Enami* reveals that *Enami* also fails to teach or suggest the last limitation of independent claim 9.

Specifically, the last limitation of independent claim 9 is each individual signal processing circuit being associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on the substrate. This limitation is neither taught nor suggested by *Enami* by the disclosure of an order in which the signal processing circuits of data line driver 40 are arranged physically on the substrate in exactly the same physical order of the signal bus lines to which the signal processing circuit blocks of data line driver 40 are respectively connected as evidenced by the following illustration of data line driver 40, wherein n = 9 for nine (9) signal processing circuits SPC1-SPC9 and nine (9) signal bus lines d1-d9.



This is identical to the teachings of the prior art illustrated in FIG. 3 of the present application. Thus, *Enami* is nothing more than a cumulative reference as to teaching an order in which signal processing circuits are arranged physically on the substrate in exactly the same physical order of the signal bus lines to which the signal processing circuit blocks are respectively connected.

Similarly, multiplexor 38 of *Enami* as shown in FIG. 1 is no more cumulative than multiplexor 31 illustrated in FIG. 2 of the present application where address conductors d1A-dnA of *Enami* are synonymous with the address conductors C1-C9 of the present application for n = 9, address conductors d1B-dnB of *Enami* are synonymous with the address conductors C10-C18 of the present application for n = 9, and so on and so on. Moreover, multiplexor 38 of *Enami* is unrelated to the last limitation of independent claim 9.

In summary, *Chang* fails to teach signal processing circuits 245_1 and 245_2 as being adjacent of a substrate. *Enami* is clearly synonymous with the FIG. 3 prior art of the present application whereby signal processing circuits 42(1)-42(9) are arranged physically on the substrate in exactly the same physical order of the signal bus lines V1-V9 to which the signal processing circuit blocks 42(1)-42(9) are respectively connected, and with the FIG. 2 prior art of the present application in the context of multiplexers. The last limitation of independent claim 9 is directed to FIGS. 4 and 5 of the present application, and therefore the combination of *Chang* in view of *Enami* unequivocally fails to teach the last limitation of independent claim 9.

Additionally, *Chang* teaches away from the last limitation of independent claim 9 by teaching a sequential control by a shift register 230 of the switches A1, A2, B1 and B2 of each signal processing circuit 245_1 to 245_{40} that is simplified based on the sequential arrangement of signal processing circuit 245_1 to 245_{40} as shown in FIG. 3. .

Withdrawal of the rejection of independent claim 9 under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of *Enami* is therefore respectfully requested.

Claim 10 depends from independent claim 9. Therefore, dependent claim 10 includes all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claim 10 is allowable over *Chang* in view of *Enami* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Chang* in view of *Enami*. Withdrawal of

the rejection of dependent claim 10 under 35 U.S.C. §103(a) being unpatentable over *Chang* in view of *Enami* is therefore respectfully requested.

B. Examiner Shapiro rejected claim 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Chang* et al. in view of U.S. Patent No. 5,892,493 to *Enami* et al. and in further view of U.S. Patent No. 6,384,806 to *Matsueda* et al.

Claim 12 depends from independent claim 9. Therefore, dependent claim 12 includes all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claim 12 is allowable over *Chang* in view of *Enami* and in further view of *Matsueda* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Chang* in view of *Enami*. Withdrawal of the rejection of dependent claim 12 under 35 U.S.C. §103(a) being unpatentable over *Chang* in view of *Enami* and in further view of *Matsueda* is therefore respectfully requested.

C. Examiner Shapiro rejected claim 13 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Chang* et al. in view of U.S. Patent No. 6,384,806 to *Matsueda* et al.

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of claim 13 over *Chang* in view of *Matsueda*. The Applicant has also thoroughly read *Chang* and *Matsueda*. To warrant this 35 U.S.C. §103(a) rejection of claim 13, all the claim limitations recited in independent claim 13 must be taught or suggested by the combination of *Chang* and *Matsueda*. See, MPEP §2143. The Applicant respectfully traverses this §103(a) rejection of claim 13, because neither *Chang* nor *Matsueda* disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein an order in which said signal processing circuits are arranged physically on said substrate is at least partially different than a

physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected" as recited in independent claim 13.

As to the traversal, Examiner Shapiro has correctly recognized *Chang*'s failure to teach or suggest the last limitation of independent claim 9. Specifically, as illustrated in FIGS. 3 and 4, *Chang* teaches signal processing circuit 245_1 to 245_{40} where signal processing circuit 245_1 is associated with the first address conductors PIX1, PIX41, PIX81, PIX121, PIX161, PIX201, PIX241, PIX281, PIX321, PIX361, PIX401, PIX441, PIX481, PIX521, PIX561 and PIX601 of groups 1-16, respectively, and where signal processing circuit 245_{40} is associated with the last address conductors PIX40, PIX80, PIX120, PIX160, PIX200, PIX240, PIX280, PIX320, PIX360, PIX400, PIX440, PIX480, PIX520, PIX560, PIX600 and PIX640 of groups 1-16, respectively. *Chang*'s fails to teach or suggest the last limitation of independent claim 9 by teaching signal processing circuit 245_1 and signal processing circuit 245_{40} are not adjacent as shown in FIG. 3.

Thus, *Matsueda* must teach or suggest the last limitation of independent claim 9 in order to establish a prima facie case of obviousness.

The video bus lines V1-V9 (FIGS. 2-5) of the present invention are taught by *Matsueda* as a 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), a 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). The teaching of the aforementioned bus lines arguably implies an existence of signal processing circuits for providing the 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), an existence of signal processing circuits for providing the 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and an existence of signal processing circuits for providing signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). However, if they exist, these implied signal processing circuits are not illustrated in FIGS. 15-17 of *Matsueda*, and more importantly, *Matsueda* fails to provide any teachings related to the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively. This is particular

evidenced by the failure of *Matsueda* to state any display quality problem related to the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively.

Thus, at best, the physical order of these implied signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B, respectively, must be deemed to be no more than cumulative to the prior art illustrated in FIG. 3 of the present invention.

Furthermore, Examiner Shapiro's assertion that column 20, lines 29-45 of *Matsueda* teaches the last limitation of independent claim 13 is erogenous, because that portion of *Matsueda* is related to capacitive lines 43 in the context of scanning lines 42, which are unrelated to the last limitation of independent claim 13.

Additionally, *Chang* teaches away from the last limitation of independent claim 9 by teaching a sequential control by a shift register 230 of the switches A1, A2, B1 and B2 of each signal processing circuit 245_1 to 245_{40} that is simplified based on the sequential arrangement of signal processing circuit 245_1 to 245_{40} as shown in FIG. 3.

Withdrawal of the rejection of independent claim 13 under 35 U.S.C. §103(a) as being unpatentable over *Chang* in view of *Matsueda* is therefore respectfully requested.

SUMMARY

Examiner Shapiro's rejection of claims 9, 10 and 12 have been obviated by the remarks herein supporting an allowance of pending claims 9, 10 and 12 over *Chang* in view of *Enami*. Examiner Shapiro's rejection of claim 13 have been obviated by the remarks herein supporting an allowance of pending claim 13 over *Chang* in view of *Matsueda*. The Applicant respectfully submits that claims 9-13 as listed herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Shapiro is respectfully requested to contact the undersigned at the telephone number listed below.

Dated: **January 24, 2005**

Respectfully submitted,
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